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A 0.20–2.43 GHz fractional-*N* frequency synthesizer with optimized VCO and reduced current mismatch CP*

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Abstract: A 0.20–2.43 GHz fractional-*N* frequency synthesizer is presented for multi-band wireless communication systems, in which the scheme adopts low phase noise voltage-controlled oscillators (VCOs) and a charge pump (CP) with reduced current mismatch. VCOs that determine the out-band phase noise of a phase-locked loop (PLL) based frequency synthesizer are optimized using an automatic amplitude control technique and a high-quality factor figure-8-shaped inductor. A CP with a mismatch suppression architecture is proposed to improve the current match of the CP and reduce the PLL phase errors. Theoretical analysis is presented to investigate the influence of the current mismatch on the output performance of PLLs. Fabricated in a TSMC 0.18-μm CMOS process, the prototype operates from 0.20 to 2.43 GHz. The PLL synthesizer achieves an in-band phase noise of −96.8 dBc/Hz and an out-band phase noise of −122.8 dBc/Hz at the 2.43-GHz carrier. The root-mean-square jitter is 1.2 ps under the worst case, and the measured reference spurs are less than −65.3 dBc. The current consumption is 15.2 mA and the die occupies 850 μm×920 μm.

Key words: Frequency synthesizer; Charge pump (CP); Voltage-controlled oscillator (VCO); Current mismatch; Phase noise
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1 Introduction

Fractional-*N* phase-locked loop (PLL) based frequency synthesizers have gained popularity in multi-band wireless communication systems as local oscillators (de Muer and Steyaert, 2002; Temporiti et al., 2004; Hedayati et al., 2009). A critical challenge in PLL synthesizers is to achieve a wide output frequency range together with low spurs and low phase noise. Spurs can create a reciprocal mixing problem (Gao et al., 2010), and poor phase noise would degrade the noise floor and the selectivity of a multi-standard reconfigurable transceiver.

Much research has been done to reduce the phase noise and enlarge the frequency range of the PLL synthesizer. In Hara et al. (2010) and Deng et al. (2012, 2014), injection locking techniques were used to achieve high-performance PLLs which suffer from limited fractional resolution and large spurs caused by a periodic hard refresh. Digital PLLs are increasingly used because of the tolerance in the low supply voltage and device leakage (Chang HH et al., 2008; Hsu et al., 2008; Liao et al., 2017; Wu et al., 2017), whereas the spurious tone and phase noise performances are inferior to that of the analog PLLs. In Chang WS et al. (2014), Narayanan et al. (2016), Sharkia et al. (2018), and Zhang et al. (2019), sub-sampling PLLs were employed to realize low phase noise, but the limited acquisition range in frequency and the difficulty in integration have prevented them from being widely used in transceivers. A classical charge pump (CP) PLL architecture (Nuzzo et al., 2009; Osmany et al., 2010; Yu SA et al.,

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2011) is always the most widely implemented in fractional-N synthesizers to meet the multi-standard application requirements of low phase noise, wide frequency range, and low spurs.

In view of the studies mentioned above, the conventional CP PLL topology is employed in this study. To reduce the in-band CP noise and out-band oscillator noise, a reduced current mismatch CP and a high-performance voltage-controlled oscillator (VCO) are proposed. The presented PLL achieves a frequency range of 0.20–2.43 GHz, low spurs, and low phase noise.

2 The proposed VCO topology

VCO is one of the key components in PLLs. To apply VCOs to multi-band wireless communication systems, it is highly desirable to keep the frequency range of the VCO as wide as possible. Moreover, VCO needs to achieve low phase noise and low power consumption. Several methods, such as the active-core transistor switching technique (Yoon et al., 2014), inductive tuning, and transformer (Ruippo et al., 2010; Italia et al., 2012), have been employed to design wideband VCOs, but suffer from limited phase noise performance. To realize wideband output together with low VCO gain and high performance, two VCO cores with similar topologies are designed and used in this study.

In a wideband VCO design, the quality factor of the inductor (Q_{ind}) has a great influence on the startup constraints and phase noise. A higher Q_{ind} makes the VCO more likely to start up and gives lower phase noise. In addition, with the complemetary metal-oxide semiconductor (CMOS) technology scaling down, the magnetic coupling problems could no longer be ignored in circuits that include inductors. Therefore, the design of a high-quality-factor inductor with enhanced isolation is a matter of cardinal significance.

On the other hand, the steady-state oscillation amplitude is important in wideband VCO design. A small amplitude restricts the phase noise performance, while a large one makes the VCO operate in a voltage-limited mode, which causes unnecessary power consumption and degradation in phase noise. Furthermore, a large amplitude variation in wideband VCOs complicates the design of blocks which are connected to the end of a VCO in a PLL. Thus, for practical designs, we need to find some solutions to control the amplitude.

In this study, an automatic amplitude control (AAC) technique is employed in the VCO core to help sustain an optimal amplitude across the tuning band. Meanwhile, an optimized high-quality-factor figure-8-shaped inductor is used to ameliorate phase noise and reduce magnetic coupling.

The proposed low-phase-noise wideband VCO is illustrated in Fig. 1. The start-up condition is described as

$$g_{\mathrm{m}} \geq \frac{\alpha}{\omega_{\mathrm{osc}} L Q_{\mathrm{ind}}}, \tag{1}$$

where g_{m} represents the transconductance, L the inductance, α the design margin factor, and ω_{osc} the oscillation frequency. The maximum g_{m} is needed on the low end of the tuning band. There is significant excess in g_{m} in the high end of the tuning band when g_{m} is fixed across the tuning range. The redundant g_{m} would cause extra power consumption, and two operating regions should be discussed (Berny et al., 2005).

A wideband VCO works in a current-limited mode over the lower portion of the frequency band

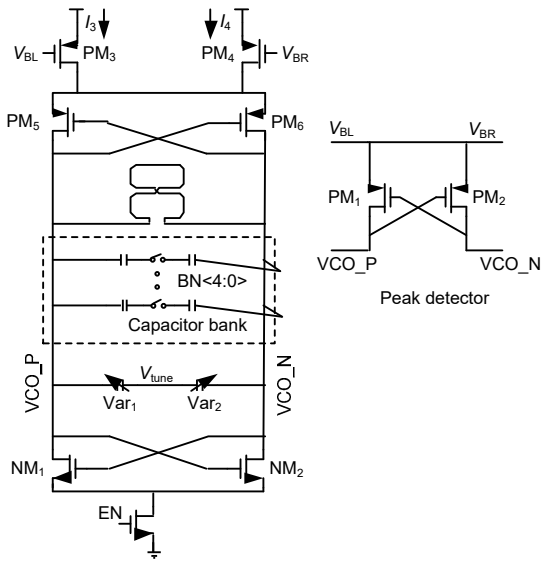

Fig. 1 The proposed voltage-controlled oscillator (VCO) with an automatic amplitude control (AAC) circuit and a figure-8-shaped inductor

and operates in a voltage-limited mode over the higher portion of the tuning band. In the current-limited mode, the phase noise is inversely proportional to the amplitude. When the amplitude is excessive and the VCO works in the voltage-limited mode, the phase noise would increase rather than decrease, as illustrated in Fig. 2a. As a result, an AAC circuit composed of PM_1–PM_4 is used. The peak detector realized by PM_1 and PM_2 detects the upper peak voltage of the VCO to control I_3 and I_4. When the amplitude goes up, the large peak voltage makes I_3 and I_4 go down to decrease the amplitude, as shown in Fig. 2b. Thus, the VCO can be prevented from working in a voltage-limited mode. Fig. 3 shows the simulated phase noise with and without the AAC circuit, in which the phase noise at the high end of the tuning band is reduced by up to 3.4 dBc/Hz with the AAC circuit. The proposed AAC circuit helps the VCO core operate in the upper edge of the current-limited region for optimal phase noise performance over the whole tuning range.

With the CMOS technology scaling down, the magnetic coupling has significant effects on the circuit blocks due to the widely used on-chip inductors (Mahmoud et al., 2016). A figure-8-shaped inductor is adopted to reduce the coupling because the magnetic fields in the two loops of the figure-8-shaped inductor are opposite and tend to cancel out each other. To prove the effectiveness of the figure-8-shaped inductor in coupling reduction, the coupling evaluated by S_{21} is simulated in two different configurations. As shown in Fig. 4a, two 550-pH conventional octagonal inductors make up configuration A. In configuration B, a 550-pH octagonal inductor and a 550-pH figure-8-shaped inductor are used. The separation distance between these two inductors in each configuration is 500 μm. Fig. 4b illustrates the simulated

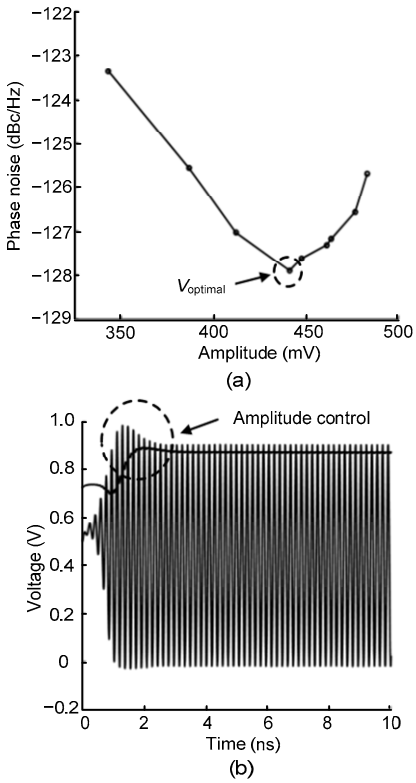

Fig. 2 Phase noise vs. amplitude at 1 MHz (a) and simulated transient of VCO (b)

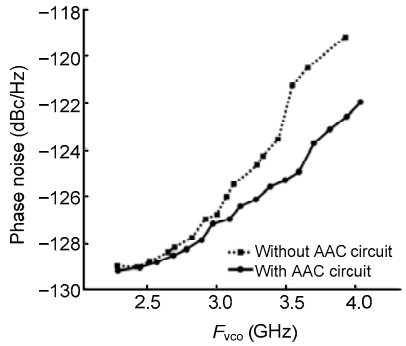

Fig. 3 Simulated VCO phase noise at 1 MHz with and without AAC circuit

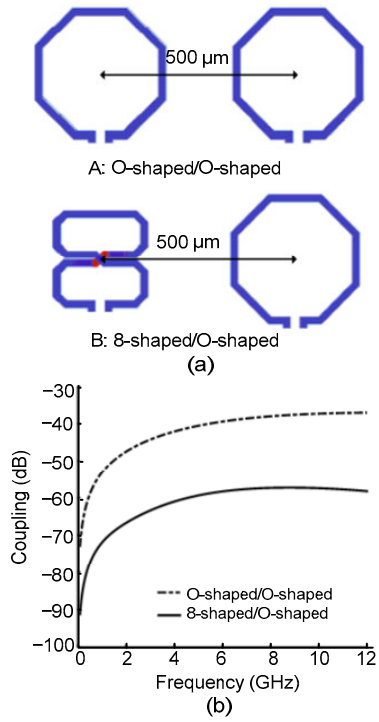

Fig. 4 Two different configurations (a) and coupling comparison (b)

coupling results, and the coupling reduction of 19.3 dB is realized at 2.6 GHz using a figure-8-shaped inductor.

On the other hand, Q_{ind} must be high enough to optimize the phase noise and relax the start-up condition (Lim et al., 2016). Therefore, a metal paralleling technique is used to increase the quality factor of the figure-8-shaped inductor. A three-dimensional inductor layout view of the used figure-8-shaped inductor is shown in Fig. 5. Metal 6 and metal 5 are used for the main coils, and metal 4 and metal 3 are employed for the cross-point sections. The measured inductance is 550 pH and the quality factor reaches 20.1 at 4.8 GHz.

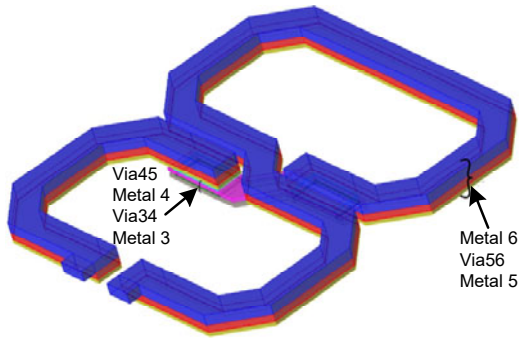

Fig. 5 Three-dimensional inductor layout view of the used figure-8-shaped inductor

The high-band VCO (VCO_H) and the low-band VCO (VCO_L) have similar topologies. Different from the metal-insulator-metal (MIM) capacitor employed in the VCO_L, the switched capacitor bank in the VCO_H is designed using N-channel metal-oxide semiconductor (NMOS) capacitors for comparison. Using the strategies investigated above, the VCO_L achieves 2.24–3.96 GHz wideband output, while the VCO_H operates from 3.20 to 4.86 GHz and the phase noise is lower than −117.7 dBc/Hz.

3 The proposed CP with reduced current mismatch

CP, which is a key component of most PLLs, introduces significant non-ideal effect of current mismatch. In integer-N PLLs, the current mismatch causes reference spurs. Nonlinearity is introduced by the current mismatch in a fractional-N PLL, which creates fractional spurs and worsens in-band noise. Several methods have been employed to improve the current match of CPs. A successive approximation register (Liang et al., 2008; Yu YH et al., 2018) and a signed counter (Jeong et al., 2013) have been used to calibrate the current mismatch, but these techniques require a long time and it is difficult to compensate for the changeable phase errors in fractional-N PLLs using these techniques. In Huh et al. (2005) and Chiu et al. (2009), a digital controller and a replica CP have been used to improve the current match, but a mismatch that limits the improvement exists between the main and the replica CPs. We propose a CP circuit with two rail-to-rail operational amplifiers to address the above-mentioned issues, resulting in perfect current match characteristics that are highly beneficial to the optimizations in in-band noise and spurs.

3.1 Analysis of current mismatch

A conventional CP and phase frequency detector (PFD) are illustrated in Fig. 6a. The phase difference between the reference clock (F_{REF}) and the feedback divider output (F_{DIV}) is detected by the PFD, and the outputs of UP and DN are generated to regulate the CP. As described in Fig. 6b, the rising edges of UP and DN occur at the rising edges of F_{REF} and F_{DIV}, and the falling edges of UP and DN occur at the point when the later rising edge goes through a delay of T_{D}. The delay should be of a proper value to avoid a dead zone and to minimize the CP output current ripple. The sourcing current (I_{UP}) and sinking current (I_{DN}) are nominally equal; however, in practice, the non-ideal factors, such as the finite output impedances, different dropping voltages, and component mismatches, result in mismatch. Assuming that the CP current mismatch is ΔI_{CP}, then

$$\begin{cases} I_{\text{UP}} = I_{\text{CP}} + \Delta I_{\text{CP}}/2, \\ I_{\text{DN}} = I_{\text{CP}} - \Delta I_{\text{CP}}/2, \end{cases} \tag{2}$$

where I_{CP} is the average of I_{UP} and I_{DN}. During the nth reference period, ΔT_n represents the time difference between the F_{REF} and F_{DIV} rising edges. The charge carried by $i_{\text{CP}}(t)$ is expressed as

$$Q_{\text{CP}}[n] = \Delta T_n I_{\text{CP}} + T_{\text{D}} \Delta I_{\text{CP}} + \left|\Delta T_n\right| \frac{\Delta I_{\text{CP}}}{2}. \tag{3}$$

The desired CP output is described by the right-hand first term of Eq. (3). The right-hand second

term of Eq. (3) is a constant error resulting from the mismatch of I_{UP} and I_{DN}, which is the main cause of the reference spur. The right-hand third term of Eq. (3) is nonlinear, and would worsen in-band noise and induce fractional spurs (Wang et al., 2008). A pedestal-based linearization technique used in Pamarti et al. (2004) can introduce an additional charge to cancel out the right-hand third term, but suffers from degradation in reference spurs and phase noise. Referring to Eq. (3), an effective method is to eliminate ΔI_{CP}, which could effectively improve CP linearity and significantly reduce different kinds of spurs and phase noise.

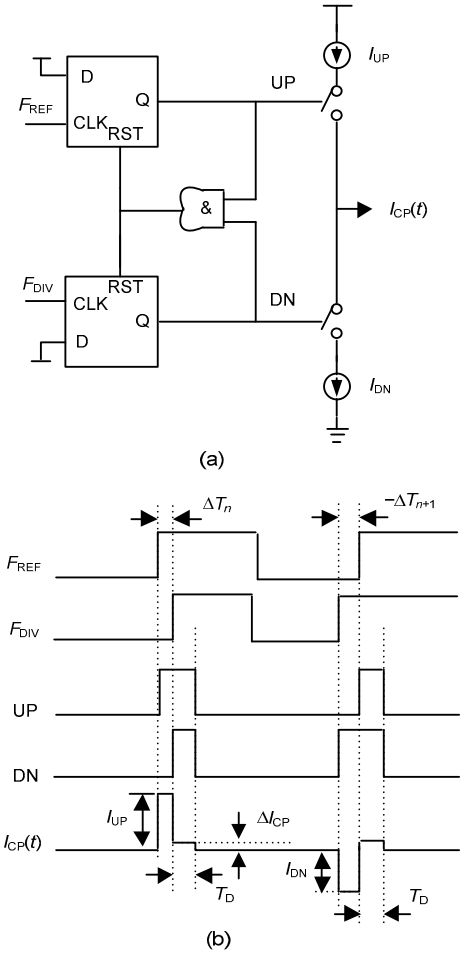

Fig. 6 Conventional phase frequency detector (PFD) and charge pump (CP) (a) and time diagram (b)

3.2 CP design

The architecture of the proposed CP is sketched in Fig. 7. The CP is driven by differential outputs of a conventional PFD, in which the complementary input switches minimize clock feed-through and charge injection. The current mirrors are made up of transistors MP_1–MP_4 and MN_1–MN_3. Two rail-to-rail operational amplifiers, Opa_1 and Opa_2, are used to maintain the current match as V_{out} changes. As indicated in Fig. 7, V_{out} and V_1 are exactly equal as a result of the clamping function of Opa_1, so the match between the sinking and sourcing currents can be guaranteed. Assuming that V_{out} increases and that the output of Opa_1 decreases, then the gate voltage of MN_1 decreases. I_1 decreases with a decrease of gate voltage, causing I_2 to be larger than I_1 and a part of I_2 to flow into Opa_1. Meanwhile, the gate voltage of MN_2 decreases, bringing an increase of V_1, and then the output of Opa_1 increases. Due to the dynamic feedback calibration, the output of Opa_1 will be stable and no current flows into Opa_1; thus, I_2 and I_1 are equal again. Because I_{UP} and I_{DN} are mirrored from I_2 and I_1, respectively, I_{UP} will match I_{DN} well when V_{out} changes. Moreover, a negative feedback loop and a positive loop are simultaneously introduced by Opa_1, and a capacitor of C_0 is therefore employed to stabilize the loop. Opa_2 is used as a unity-gain amplifier to minimize the charge sharing, which may cause ripples in the CP output voltage. The rail-to-rail structure is used in Opa_1 and Opa_2 to achieve current match over a large output voltage range. The other transistors biased at power or ground are employed for device match.

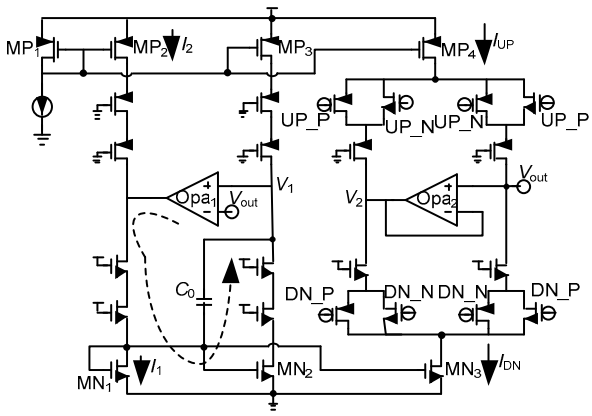

Fig. 7 The proposed CP topology

With all the designs investigated above, I_{UP} and I_{DN} achieve perfect match. Fig. 8 illustrates the simulated gain of the PFD and CP. The input frequency is 24 MHz and the CP current is 300 μA. By simulating the average CP output current as a function of the

phase error at the PFD input and by differentiating the result, the gain is calculated. The slope of the gain curve is approximately −0.65 μA/rad^2, showing good CP linearity. Fig. 9 shows the simulated match characteristics. The sourcing and sinking currents match well within a CP output voltage range of 0.15–1.64 V. With a current of 100 μA, the CP approaches current mismatch of less than 0.16%, which is highly beneficial to spurs and in-band noise. Fig. 10 shows the Monte-Carlo simulation results of the match characteristics including the effect of device mismatch and process variation at 27 °C. The current mismatch shows a standard deviation of 313 nA and a mean value of −27 nA involving 500 samples, which indicates that the current mismatch of 93% of samples is less than ±0.55%. Table 1 gives the current mismatch at typical (TT), fast (FF), and slow (SS) process corners with supply voltage and temperature variations. As we can see in Table 1, the current mismatch is less than ±0.25% with the influences of process spread and the fluctuation of temperature and supply voltage.

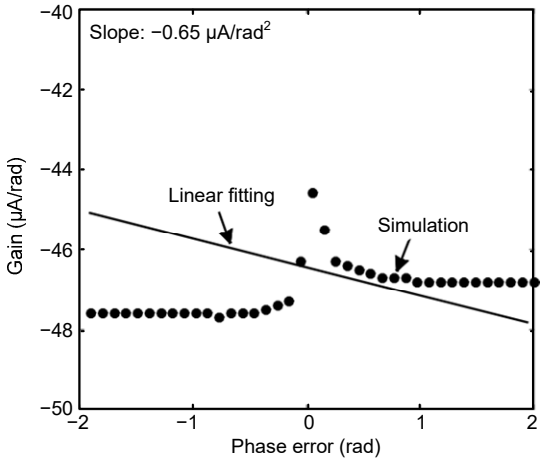

Fig. 8 Simulated gain vs. input phase error

4 Low-phase-noise wideband-frequency synthesizer

Fig. 11 illustrates the top architecture of the proposed PLL synthesizer. The structure of the PFD is the same as that in Fig. 6, which is made up of several necessary D-flip flops (DFFs) and logic gates. DFFs

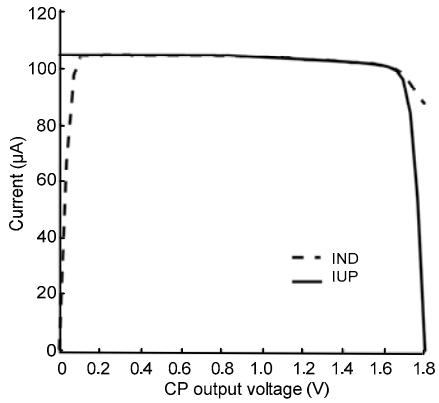

Fig. 9 Simulated current match characteristics with a 1.8-V supply and a typical process corner (TT)

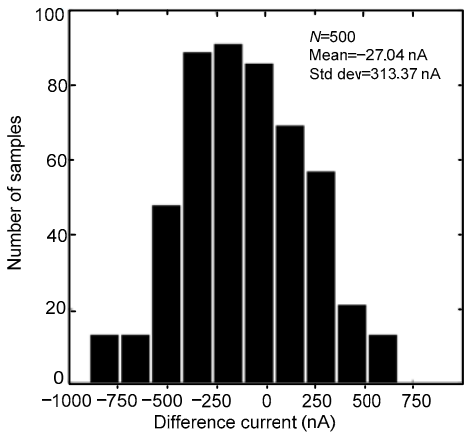

Fig. 10 Monte-Carlo simulation results of match characteristics

Table 1 Current mismatch with the variation of process corners, supply voltage, and temperature

Corner.volt.temp.	ΔI_{CP} (%)	Corner.volt.temp.	ΔI_{CP} (%)	Corner.volt.temp.	ΔI_{CP} (%)
TT.1.62V.−45°C	−0.11	SS.1.62V.−45°C	−0.02	FF.1.62V.−45°C	−0.22
TT.1.62V.27°C	−0.14	SS.1.62V.27°C	−0.05	FF.1.62V.27°C	−0.13
TT.1.62V.125°C	−0.07	SS.1.62V.125°C	−0.06	FF.1.62V.125°C	−0.06
TT.1.8V.−45°C	−0.24	SS.1.8V.−45°C	−0.03	FF.1.8V.−45°C	−0.11
TT.1.8V.27°C	−0.16	SS.1.8V.27°C	−0.04	FF.1.8V.27°C	−0.08
TT.1.8V.125°C	−0.04	SS.1.8V.125°C	−0.06	FF.1.8V.125°C	−0.06
TT.1.98V.−45°C	−0.13	SS.1.98V.−45°C	−0.25	FF.1.98V.−45°C	−0.07
TT.1.98V.27°C	−0.06	SS.1.98V.27°C	−0.13	FF.1.98V.27°C	−0.04
TT.1.98V.125°C	−0.02	SS.1.98V.125°C	−0.04	FF.1.98V.125°C	0.03

are designed using a true-single-phase-clock structure to save power and reduce the die size. A simple interface circuit, in which a single-ended signal is converted into differential signals, exists between PFD and CP. The two-core VCO tunes from 2.24 to 4.86 GHz. A MASH-1-1-1 Delta-Sigma modulator (DSM) and a multi-modulus divider (MMD) are used to achieve fractional frequency division. Instead of the pulse swallow divider architecture, the divide-by-2/3 cells are used for a wide division range and low power consumption. Moreover, the divider ratio dithering achieved by the MASH-1-1-1 DSM with an MMD reduces the quantization noise and consequently further suppresses the in-band phase noise. An output divider with a division ratio of M (M=2/4/8/16) is used between the PLL output and the VCO output, which doubles the VCO frequency and thus avoids the pulling effect from the power amplifier (PA) in the transceiver. Meanwhile, the output divider is employed to enlarge the PLL output frequency range and provide the mixer with quadrature local oscillation signals. An automatic frequency control block is used to realize coarse tuning, which has not been displayed in Fig. 11 for brevity.

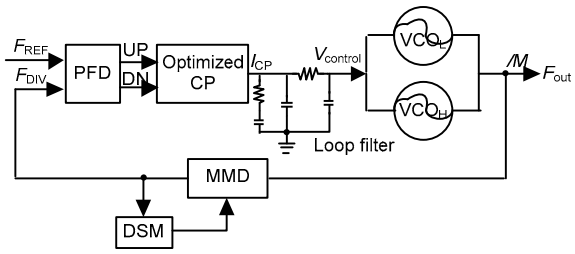

Fig. 11 Implemented fractional-*N* PLL

5 Measurement results

A PLL synthesizer using the proposed VCO and CP is fabricated in a TSMC 180-nm CMOS process. A die photomicrograph with an integrated loop filter is shown in Fig. 12, and the die size is 850 μm× 920 μm. To reduce the noise coupling between the digital blocks and the VCO, vertical guard rings are employed. The measurements are carried out using a low-noise crystal oscillator of 24 MHz as a reference clock.

The measured VCO tuning curves are illustrated in Fig. 13 with the tuning voltage changing from 0.30 to 1.50 V. The measured frequency band of VCO_H is 3.20–4.86 GHz, and the frequency of VCO_L varies from 2.24 to 3.96 GHz. The measured phase noise and simulated phase noise of VCO_L and VCO_H are illustrated in Fig. 14, and the largest phase noise is −117.7 dBc/Hz at the 4.86 GHz carrier.

The measured output spectra at 0.72 and 2.43 GHz are shown in Fig. 15. At 0.72 GHz, the level of reference spur is as low as −72.2 dBc. The reference spur and fractional spur at 2.43 GHz are −65.3

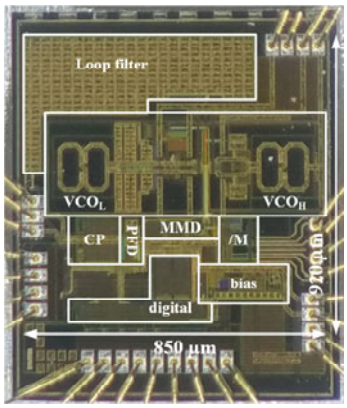

Fig. 12 Chip photograph of the synthesizer

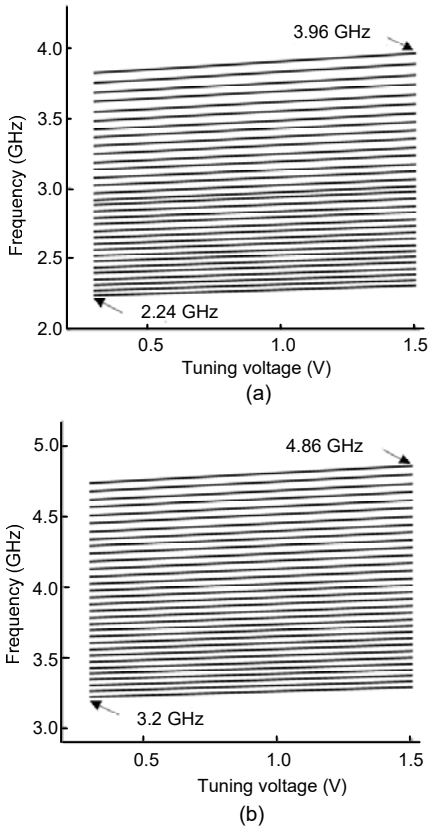

Fig. 13 Measured VCO tuning curves: (a) VCO_L; (b) VCO_H

and −79.8 dBc, respectively. The measured PLL phase noise is shown in Fig. 16. At 2.43 GHz, the phase noise is −122.8 dBc/Hz at 1 MHz offset and −96.8 dBc/Hz at 10 kHz. The phase noise at 0.72 GHz is −133.6 dBc/Hz at 1 MHz offset, and a phase noise of −106.2 dBc/Hz is achieved at 10 kHz offset. The root-mean-square (RMS) jitters are about 0.62 and 0.96 ps at 0.72 and 2.43 GHz, respectively. Fig. 17 shows the measured RMS jitter and spot phase noise over the 0.20–2.43 GHz frequency band, in which the spot phase noise at 1 MHz offset is −122.8 dBc/Hz under the worst case and the RMS jitter is below 1.2 ps. The proposed CP and VCO with lower noise are beneficial to the in-band and out-band noise, respectively. The measured out-band fractional spurs are less than −71 dBc, and the measured less-attenuated in-band fractional spurs are less than −50 dBc. Fig. 18 shows the reference spurs over the working band, which are less than −65.3 dBc. Table 2 summarizes the chip characteristics and provides comparisons with other PLL synthesizers. Using the proposed VCO and CP, the proposed PLL synthesizer achieves a wide output frequency range, low phase noise, and comparable figure of merit.

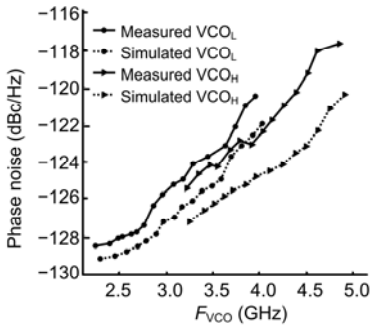

Fig. 14 Simulated phase noise and measured phase noise of VCO$_L$ and VCO$_H$

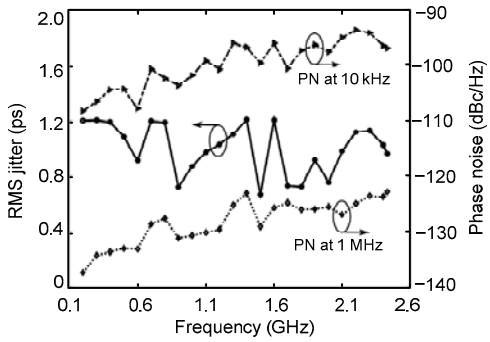

Fig. 17 Measured RMS jitter and spot phase noise over the 0.20–2.43 GHz frequency band

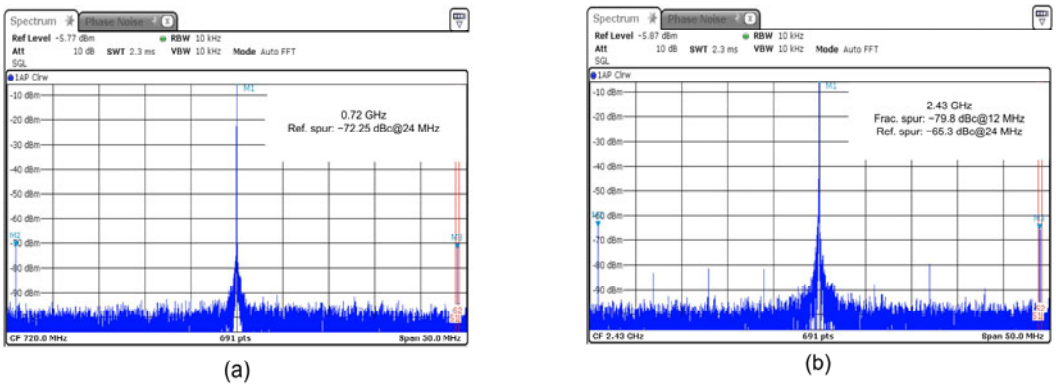

Fig. 15 Measured output spectra at 0.72 GHz (a) and 2.43 GHz (b)

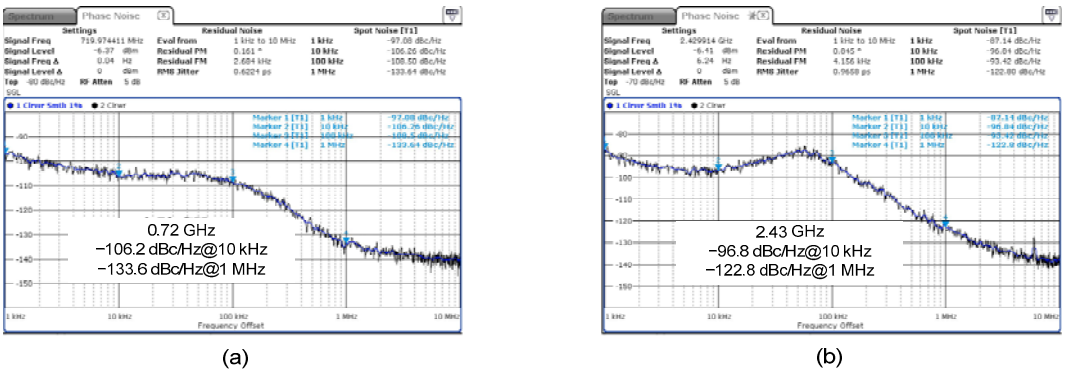

Fig. 16 Measured phase noise of the PLL synthesizer at 0.72 GHz (a) and 2.43 GHz (b)

Table 2 PLL performance comparison

Reference	CMOS process (nm)	Freqency tuning range (GHz)	F_{REF} (MHz)	Phase noise	Jitter (ps)	Reference spur (dBc)
Deng et al. (2014)	65	0.01–6.60	36	−135.3 dBc@3 MHz		−79
Wu et al. (2017)	40	1.73–3.38	50	−109 dBc@100 kHz	0.42	
Chang WS et al. (2014)	180	2.12–2.40	48	−134.8 dBc@10 MHz	0.26	−55
Narayanan et al. (2016)	65	4.34–4.94	40	−131.8 dBc@10 MHz	0.13	−70.8
This paper	180	0.20–2.43	24	−122.8 dBc@1 MHz	0.96	−65.3

Reference	In-band fractional spur (dBc)	Out-band fractional spur (dBc)	Power (mW)	FOM[a] (dB)	FOMT[b] (dB)
Deng et al. (2014)			16–26	177.3	−203.3
Wu et al. (2017)	−42		10.7	184.7	−200.9
Chang WS et al. (2014)	−48	−70	17.3	169.6	−171.5
Narayanan et al. (2016)	−59.2	−75	6.2	177.7	−179.9
This paper	−50	−71	27.3	176.1	−200.7

a: $\mathrm{FOM} = 10\lg\left[\left(\frac{f_0}{\Delta f}\right)^2\left(\frac{1\,\mathrm{mW}}{\mathrm{power}}\right)\right] - L(\Delta f)$; b: $\mathrm{FOMT} = L(\Delta f) - 20\lg\left(\frac{f_0}{\Delta f}\frac{\mathrm{FTR}}{10}\right) + 10\lg\left(\frac{\mathrm{power}}{1\,\mathrm{mW}}\right)$

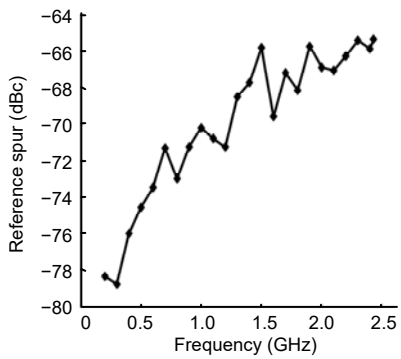

Fig. 18 Measured reference spur vs. output frequency

6 Conclusions

A low phase noise wideband fractional-*N* phase-locked loop (PLL) synthesizer with an optimized voltage-controlled oscillator (VCO) and a charge pump (CP) has been presented. An automatic amplitude control (AAC) technique and a high-quality-factor figure-8-shaped inductor have been used to improve the performance of the proposed VCO. A circuit architecture that flexibly adopts two rail-to-rail operational amplifiers has been proposed to improve the CP current match and the linearity. Using the techniques mentioned in this study, the spot phase noise at 1 MHz offset was −122.8 dBc/Hz under the worst case, the root-mean-square (RMS) jitter was below 1.2 ps within the whole 0.20–2.43 GHz output range, and the reference spurs were less than −65.3 dBc.

Contributors

Wei ZOU designed the research and drafted the manuscript. Daming REN processed the data and helped organize the manuscript. Wei ZOU and Xuecheng ZOU revised and finalized the paper.

Compliance with ethics guidelines

Wei ZOU, Daming REN, and Xuecheng ZOU declare that they have no conflict of interest.

References

Berny AD, Niknejad AM, Meyer RG, 2005. A 1.8-GHz LC VCO with 1.3-GHz tuning range and digital amplitude calibration. *IEEE J Sol-State Circ*, 40(4):909-917. https://doi.org/10.1109/JSSC.2004.842851

Chang HH, Wang PY, Zhan JHC, et al., 2008. A fractional spur-free ADPLL with loop-gain calibration and phase-noise cancellation for GSM/GPRS/EDGE. IEEE Int Conf on Solid-State Circuits, p.200-201, 606. https://doi.org/10.1109/ISSCC.2008.4523126

Chang WS, Huang PC, Lee TC, 2014. A fractional-N divider-less phase-locked loop with a subsampling phase detector. *IEEE J Sol-State Circ*, 49(12):2964-2975. https://doi.org/10.1109/JSSC.2014.2359670

Chiu WH, Chang TS, Lin TH, 2009. A charge pump current missmatch calibration technique for ΔΣ fractional-*N* PLLs in 0.18-μm CMOS. IEEE Asian Solid-State Circuits Conf, p.73-76. https://doi.org/10.1109/ASSCC.2009.5357182

de Muer B, Steyaert MSJ, 2002. A CMOS monolithic ΔΣ-controlled fractional-*N* frequency synthesizer for DCS-1800. *IEEE J Sol-State Circ*, 37(7):835-844. https://doi.org/10.1109/JSSC.2002.1015680

Deng W, Musa A, Okada K, et al., 2012. A 0.38 mm^2,

10 MHz–6.6 GHz quadrature frequency synthesizer using fractional-*N* injection-locked technique. IEEE Asian Solid State Circuits Conf, p.353-356. https://doi.org/10.1109/ASSCC.2012.6570787

Deng W, Hara S, Musa A, et al., 2014. A compact and low-power fractionally injection-locked quadrature frequency synthesizer using a self-synchronized gating injection technique for software-defined radios. *IEEE J Sol-State Circ*, 49(9):1984-1994. https://doi.org/10.1109/JSSC.2014.2334392

Gao X, Klumperink EAM, Socci G, et al., 2010. Spur reduction techniques for phase-locked loops exploiting a sub-sampling phase detector. *IEEE J Sol-State Circ*, 45(9):1809-1821. https://doi.org/10.1109/JSSC.2010.2053094

Hara S, Okada K, Matsuzawa A, 2010. 10 MHz to 7 GHz quadrature signal generation using a divide-by-4/3, -3/2, -5/3, -2, -5/2, -3, -4, and -5 injection-locked frequency divider. Symp on VLSI Circuits, p.51-52. https://doi.org/10.1109/VLSIC.2010.5560270

Hedayati H, Bakkaloglu B, Khalil W, 2009. A 1 MHz-bandwidth type-I ΔΣ fractional-N synthesizer for WiMAX applications. IEEE Int Conf on Solid-State Circuits, p.390-391, 391a. https://doi.org/10.1109/ISSCC.2009.4977472

Hsu CM, Straayer MZ, Perrott MH, 2008. A low-noise, wide-BW 3.6 GHz digital ΔΣ fractional-N frequency synthesizer with a noise-shaping time-to-digital converter and quantization noise cancellation. IEEE Int Conf on Solid-State Circuits, p.340-617. https://doi.org/10.1109/ISSCC.2008.4523196

Huh H, Koo Y, Lee KY, et al., 2005. Comparison frequency doubling and charge pump matching techniques for dual-band ΔΣ fractional-N frequency synthesizer. *IEEE J Sol-State Circ*, 40(11):2228-2236. https://doi.org/10.1109/JSSC.2005.857368

Italia A, Ippolito CM, Palmisano G, 2012. A 1-mW 1.13–1.9 GHz CMOS LC VCO using shunt-connected switched-coupled inductors. *IEEE Trans Circ Syst I*, 59(6):1145-1155. https://doi.org/10.1109/TCSI.2011.2173383

Jeong CH, Kim KY, Kwon CK, et al., 2013. Digital calibration technique using a signed counter for charge pump mismatch in phase-locked loops. *IET Circ Dev Syst*, 7(6): 313-318. https://doi.org/10.1049/iet-cds.2013.0011

Liang CF, Chen SH, Liu SI, 2008. A digital calibration technique for charge pumps in phase-locked systems. *IEEE J Sol-State Circ*, 43(2):390-398. https://doi.org/10.1109/JSSC.2007.914283

Liao DY, Wang HC, Dai FF, et al., 2017. An 802.11a/b/g/n digital fractional-*N* PLL with automatic TDC linearity calibration for spur cancellation. *IEEE J Sol-State Circ*, 52(5):1210-1220. https://doi.org/10.1109/JSSC.2016.2638882

Lim CC, Ramiah H, Yin J, et al., 2016. A high-Q spiral inductor with dual-layer patterned floating shield in a class-B VCO achieving a 190.5-dBc/Hz FoM. IEEE Int Symp on Circuits and Systems, p.2759-2762. https://doi.org/10.1109/ISCAS.2016.7539164

Mahmoud A, Fanori L, Mattsson T, et al., 2016. A 2.8-to-5.8 GHz harmonic VCO based on an 8-shaped inductor in a 28 nm UTBB FD-SOI CMOS process. *Analog Integr Circ Signal Process*, 88(3):391-399. https://doi.org/10.1007/s10470-016-0759-4

Narayanan AT, Katsuragi M, Kimura K, et al., 2016. A fractional-N sub-sampling PLL using a pipelined phase-interpolator with an FoM of −250 dB. *IEEE J Sol-State Circ*, 51(7):1630-1640. https://doi.org/10.1109/JSSC.2016.2539344

Nuzzo P, Vengattaramane K, Ingels M, et al., 2009. A 0.1–5 GHz dual-VCO software-defined ΔΣ frequency synthesizer in 45 nm digital CMOS. Proc IEEE Radio Frequency Integrated Circuits Symp, p.321-324. https://doi.org/10.1109/RFIC.2009.5135549

Osmany SA, Herzel F, Scheytt JC, 2010. An integrated 0.6–4.6 GHz, 5–7 GHz, 10–14 GHz, and 20–28 GHz frequency synthesizer for software-defined radio applications. *IEEE J Sol-State Circ*, 45(9):1657-1668. https://doi.org/10.1109/JSSC.2010.2051476

Pamarti S, Jansson L, Galton I, 2004. A wideband 2.4-GHz delta-sigma fractional-NPLL with 1-Mb/s in-loop modulation. *IEEE J Sol-State Circ*, 39(1):49-62. https://doi.org/10.1109/JSSC.2003.820858

Ruippo P, Lehtonen TA, Tchamov NT, 2010. An UMTS and GSM low phase noise inductively tuned LC VCO. *IEEE Microw Wirel Compon Lett*, 20(3):163-165. https://doi.org/10.1109/LMWC.2010.2040219

Sharkia A, Mirabbasi S, Shekhar S, 2018. A 0.01 mm^2 4.6-to-5.6GHz sub-sampling type-I frequency synthesizer with –254 dB FOM. Proc IEEE Int Conf on Solid-State Circuits, p.256-258. https://doi.org/10.1109/ISSCC.2018.8310281

Temporiti E, Albasini G, Bietti I, et al., 2004. A 700-kHz bandwidth ΣΔ fractional synthesizer with spurs compensation and linearization techniques for WCDMA applications. *IEEE J Sol-State Circ*, 39(9):1446-1454. https://doi.org/10.1109/JSSC.2004.831598

Wang KJ, Swaminathan A, Galton I, 2008. Spurious tone suppression techniques applied to a wide-bandwidth 2.4 GHz fractional-N PLL. *IEEE J Sol-State Circ*, 43(12): 2787-2797. https://doi.org/10.1109/JSSC.2008.2005716

Wu Y, Shahmohammadi M, Chen Y, et al., 2017. A 3.5–6.8-GHz wide-bandwidth DTC-assisted fractional-N all-digital PLL with a MASH ΣΔ-TDC for low in-band phase noise. *IEEE J Sol-State Circ*, 52(7):1885-1903. https://doi.org/10.1109/JSSC.2017.2682841

Yoon H, Lee Y, Kim JJ, et al., 2014. A wideband dual-mode LC-VCO with a switchable gate-biased active core. *IEEE*

Trans Circ Syst II, 61(5):289-293.
https://doi.org/10.1109/TCSII.2014.2305216

Yu SA, Baeyens Y, Weiner J, et al., 2011. A single-chip 125-MHz to 32-GHz signal source in 0.18-μm SiGe BiCMOS. *IEEE J Sol-State Circ*, 46(3):598-614.
https://doi.org/10.1109/JSSC.2011.2104551

Yu YH, Chen JH, Chen YJE, 2018. A wideband 90-nm CMOS phase-locked loop with current mismatch calibration for spur reduction. IEEE Conf on Asia-Pacific Microwave, p.1504-1506.
https://doi.org/10.23919/APMC.2018.8617454

Zhang Z, Zhu G, Yue CP, 2019. 30.8 A 0.65V 12-to-16GHz sub-sampling PLL with 56.4fs_{rms} integrated jitter and −256.4dB FoM. IEEE Int Conf on Solid-State Circuits, p.488-490.
https://doi.org/10.1109/ISSCC.2019.8662378